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Pentacene-Based Organic Field-Effect Transistors: Analytical Model and Simulation Methods versus Experiment Data

M.J. Sharifi[1], A. Bazyar[2]
Faculty of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran
[1] M_j_Sharifi@sbu.ac.ir [2] a_b61712@yahoo.com

Abstract **– Organic Field-Effect Transistors, OFETs, attract much interest recently and their proficiency and hence applications are being enhanced increasingly. However, only analytical model of old field-effect transistors, developed for silicon-based transistors, and their relevant numerical analyses have been used for such devices, so far. Increasing precision of such models and numerical methods are essential now in order to modify OFETs and propose more effective models and methods. This study pegs at comparing current analytical model, simulation methods and experiment data and their fitness with each other. Certainly, four aspects of results of three abovementioned approaches were examined comparatively: sub-threshold slope, on-state drain current, threshold voltage and carrier mobility. We embark to analyze related experiment data of OFETs made by pentacene, as the organic material, along with various organic gate insulators including CyEP, PVP, PMMA, Parylene-C and Polyimide and then to offer their results, comparatively.**

Keywords: Organic Field-Effect Transistors, IEEE1620, Pentacene, ATLAS (Silvaco) simulator.

I. Introduction

Field-effect transistors' technology is being developed since its advent and it is considered as the main foundation of both electronic and information technology (IT) industries. However, during recent years, organic materials' technology and application of them to organic field-effect transistors have drawn much interest. It is because of potential capability of such transistors to realize large-scale, inexpensive, light weight and flexible electronic devices. Deposition of organic materials does not need high temperatures so such low construction temperature paves the way for their construction on inexpensive and flexible plastic substrates. In this way many applications have been proposed for organic transistors, so far. Some of them are large-scale flat displays, Radio Frequency Identification (RFID) tags, chemical sensors, etc [1].

Although mobility of some organic transistors is presently comparable or even better than amorphous silicon transistors (a-Si:H), but most organic substances still have a relatively low mobility [2]. Pentacene is an aromatic hydrocarbon which has been studied enormously because of its higher mobility amongst other organic materials. Its molecular structure is depicted on figure 1. Most of pentacene-based organic field-effect transistors act as p-channel or hole-conducting transistors [2].

Aside from mobility, there are other factors affect on performance of organic transistors. Interaction between organic substance and gate insulator plays an important role in device charge transport. Most organic transistors still use SiO_2 as the gate insulator. Nevertheless, using organic substances as gate insulators for realizing inexpensive and flexible electronic devices is highly suggested [3]. In this paper, effects of five organic gate insulators namely CyEP, PMMA, PVP, Parylene-C, and Polyimide are studied. Section 2 introduces physical structure, analytical model and numerical methods which are used for such devices conventionally. Section 3 introduces our comparative results and analysis and the conclusions.

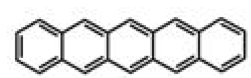

Figure 1: Molecular Structure of Pentacene [2]

II. Physical structure, analytical model and numerical methods

A. Device Structure

In this paper, organic field-effect transistors with Top-Contact configuration, in which channel width and length are 100μm and 5mm respectively, are studied [4]. A schematic structure of the mentioned transistors is depicted in figure 2.

A glass bed has been employed to construct such transistors. Indium Tin Oxide (ITO) was placed over this bed which acts as a gate electrode, then gate insulator was situated on it and pentacene organic active substance, as thick as 10 nm, was placed through thermal evaporation process. Finally, golden source and drain electrodes, as thick as 50 nm, were positioned through masking method. The specifications of used gate insulators of this study are summarized in table I.

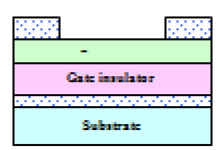

Figure 2: Top contact device structure

B. Device Simulation Techniques

Currently software which has been mostly developed to study silicon-based field-effect transistors are used to

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simulate organic transistors. In this study, we use ATLAS (Silvaco) simulator as a general software. This simulator is able to predict electrical properties of the device given its physical structure and operating bias condition by solving Poisson's and continuity equations and classic equations of carrier currents including drift and diffusion terms [5].

$$\varepsilon \nabla^2 \psi = -pq \tag{1}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \nabla . J_p + G_p - R_p \tag{2}$$

Where, ε is dielectric constant, ψ is potential profile, p is hole density, q is the unit charge, G_p is carrier generation rate, R_p is the carrier recombination rate, and J_p is the hole current density.

$$J_p = qp\mu_p F + qD_p \nabla p \tag{3}$$

Where μ_p is the mobility of holes, F is the electric field, and D_p is the hole diffusion constant.

Since ATLAS simulator has been proposed initially to simulate silicon devices, its capacity to simulate organic devices is limited in some cases as it will be seen later. Used parameters' values for pentacene in this study were as the following; Energy bandgap is 2.49 eV, electron affinity as 2.8 eV, density of both conduction and valance band states as 2×10^{21} cm^{-3} and dielectric constant as 4 [2, 7, 8]. The acceptor doping concentration of pentacene is taken 310^{16} cm^{-3} [1]. Pool-Frenkel mobility model is used for conduction channel of pentacene:

$$\mu(E) = \mu_\circ \exp\left[-\frac{\Delta}{KT} + \left(\frac{\beta}{KT} - \gamma \right) \sqrt{E} \right] \tag{4}$$

Where is the field effect dependent mobility, is the zero field mobility, is the electric field, is the zero field activation energy, is the Pool-Frenkel factor, is the fitting parameter, is the Boltzman constant, and is the temperature [3].

C. Analytical Model for Organic Field-Effect Transistors

IEEE1620 Standard has suggested that drain current of an organic transistor would be calculated using classic theory of conventional non-organic transistors [9]:

$$I_D = \frac{W}{2L} C_i \mu (V_{GS} - V_{th})^2$$

$$\text{for} \quad |V_{GS} - V_{th}| > |V_{DS}| > 0 \tag{5}$$

$$I_D = \frac{W}{L} C_i \mu (V_{GS} - V_{th}) V_{DS}$$

$$\text{for} \quad |V_{DS}| > |V_{GS} - V_{th}| > 0 \tag{6}$$

Where W and L are the channel width and channel length, C_i is the capacitance per unit area of the gate insulator, μ is the mobility, and V_{th} is the threshold voltage.

III. Results And Discussion

The extracted and the other used parameters in both the simulations and the analytical calculations in this paper, are given in tables 2 and 3. In these simulations using ATLAS software, regarding the Pool-Frenkel mobility model of pentacene, the zero field activation energy and the Pool-Frenkel factor, β, are set to 0.1 eV, and 4.35×10^{-5} ev(cm/V)$^{1/2}$ respectively and the fitting parameter, γ, was 10^{-5}(cm/V)$^{1/2}$. Regarding the interface trap state densities, their experimental values were used in the simulations [3].

In early simulations, in some cases, mismatch between experimental and simulated curves were observed. In order to resolve this problem, simulation programs must be firstly calibrated. For calibration, we should add some fixed charges at the semiconductor/oxide interface. This procedure can adjust the threshold voltage. After calibration, the electrical behavior of simulated transistors became well. At the following, we report similarities and differences exist between analytical results, simulation results and experimental data regarding the four different mentioned subjects.

Table I: Parameters and characteristics of the polymer dielectrics

Dielectric	Thickness (nm)	Dielectric constant (ε)	C_i (nF/cm^2)	Roughness (Å)
CyEP	900	18	18	28
PVP	300	5	15	6
PMMA	900	3.5	3.4	4
Parylene	600	3	4.4	48
Polyimide	400	3.3	7.3	9

A. Sub-Threshold Region

Concerning equations (5) and (6), analytical model predicts that for $V_{GS} = V_{th}$, the drain current vanishes and it will be zero for all $V_{GS} < V_{th}$. Therefore, such equations fail to measure correct value of drain current in sub-threshold region. In a better model [1], drain current in this region takes an exponential dependency to the gate-source voltage as:

$$I_D = \frac{W}{L} K \mu_{FE} C_{ox} (1 - ^{-qV_{DS}/kT}).e^{qV_{GS}/nkT} \tag{7}$$

Where, K is a constant that depends on material type and device structure, and n is an ideality factor. Both these parameters must be adjusted to match with experiment and/or simulation data.

In figure 3, transfer characteristics of sub-threshold region in logarithmic scale is shown regarding simulation method and analytical model in comparison with the experiment data. Given results of figure 3, it is concluded that sub-threshold slope of experiment data is always lower than that from simulated curves. Similarly, for sub-threshold slope of theoretical results, it is evident that their best fit, which are depicted in our figures, are different from simulation and experiment data considerably. Thus it may be concluded that eq.7 is not a proper model at all, because this equation will be

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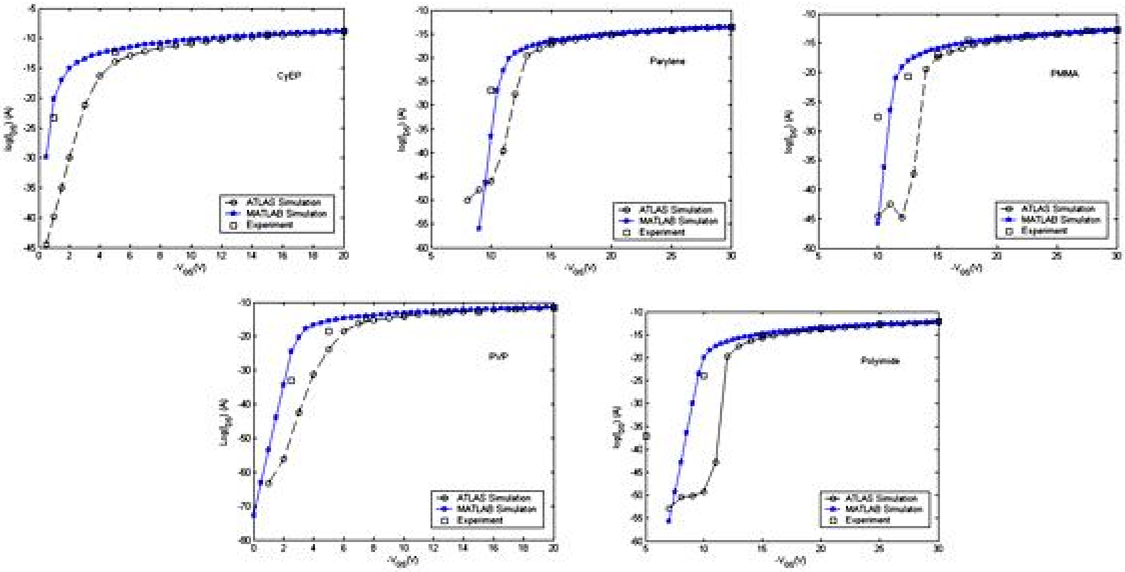

Figure 3: Transfer characteristics in logarithmic scale for studied transistors using simulation method, analytical model and experiment data

a straight line with a fixed slope in logarithmic scale and it is unlikely to develop a continuous curve in vicinity of $V_{GS} > V_{th}$ region (eq. 5, 6).

B. On-State Drain Current

Transfer characteristics of our transistors from simulation and from analytical model (equations 2 and 3) are shown in figure 4. Experiment data for such diagrams have not been in access.

As it is seen from figure 4, analytical results have been tuned so that they are matched at the beginning and the end of the bias range in each plot with the simulation results, but in spite to this, the results are not matched in intermediate gate-source voltages and simulation results always represent lower current in comparison with the analytical results. This difference may be attributed to better modeling of mobility and also due to considering horizontal and vertical fields in the simulation method in comparison with the analytical method which uses a fixed mobility and neglects the horizontal and vertical field dependencies.

C. Threshold Voltage

In analytical model, threshold voltage is a fixed value which is calculated from physical specifications of the transistor such as its insulator thickness (t_{ox}), insulator permittivity (ε_{ox}) and doping profile of semi-conductor substrate. Empirically it has been shown that various parameters affect threshold voltage of transistor and there are different values for threshold voltage in linear and saturated regions of transistor. In linear and saturation regions, threshold voltage is extracted from $I_D - V_{GS}$ and $\sqrt{I_D} - V_{GS}$ curves, respectively.

In the simulation method, threshold voltage is not a given number, but it is a value which can be calculated from the results as it is done in analytical model. Although this voltage is a function of the drain-source voltage, but, it is extracted in a certain drain-source voltage in linear and or satu rated region. There are two major reasons for threshold voltage dependency on the drain-source voltages: (a) mobility that follows the vertical field, and (b) horizontal and vertical fields interference. The former has been considered in the analytical model, but the latter is considered only in the simulation method. Tables 2 and 3 represent results of simulation method and analytical methods. It is observed that the second column of table 3 is not matched with the expected behavior. Threshold voltage can be written as the sum of two voltages as shown in fig.5.

$$V_{th} = V_1 + V_2 \tag{8}$$

Where, V_1 is part of threshold voltage due to semiconductor, and V_2 is the contribution from the insulator. V_1 is not function of the insulator parameters, therefore, we have:

$$V_{th} = V_1 + \frac{t_{ox} \cdot E_s \cdot \varepsilon_s}{\varepsilon_i} \tag{9}$$

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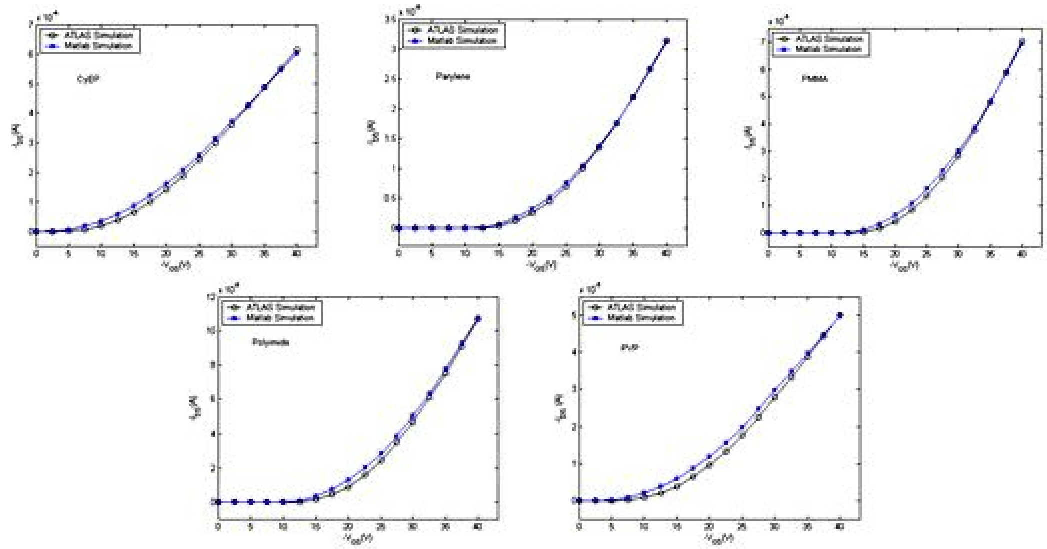

Figure 4: Transfer characteristics of the certain transistors from simulation method and analytical model

Considering the above formula, we see that, as mentioned before, the second column of tables 2 and 3 are matched neither with experimental data nor with simulation results. The reason is the interface charges exist due to interface roughness and is neglected in both approaches

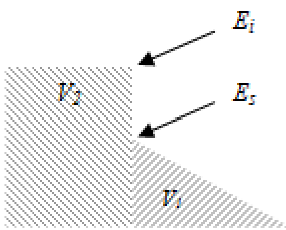

Figure 5: Potential graph in insulator/semiconductor interface

TABLE II: ELICITED RESULTS AND PARAMETERS FROM ATLAS SIMULATIONS

Dielectric	Threshold voltage (V)	Mobility ($cm^2/V.s$)	Conductivity ($\Omega^{-1}.cm^{-1}$)
CyEP	-1.1	0.90	6.2
PVP	-2.5	0.096	12
PMMA	-11	0.076	0.094
Parylene	-10.5	0.023	0.014
Polyimide	-10	0.068	3.8

TABLE III: OBTAINED RESULTS OF EXPERIMENTAL DATA

Dielectric	Threshold voltage (V)	Mobility ($cm^2/V.s$)	Conductivity ($\Omega^{-1}.cm^{-1}$)
CyEP	-1.2	0.94	6.9
PVP	-2.8	0.10	12.4
PMMA	-11.2	0.09	0.11
Parylene	-10.8	0.03	0.017
Polyimide	-9.6	0.06	3.8

D. Mobility

Mobility is considered a fixed value in the analytical model, but experimentally it has been proven that it depends on the gate-source and the drain-source voltages which are not considered in the analytical model. In fact, upon extracting the mobility from the measurement data, it should be considered as a voltage dependent quantity which is derived from small signal measurements. In the linear and saturated regions it can be calculated via eq. 10 and 11, respectively;

$$\mu_{FE} = \frac{L}{WC_{ox}V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \tag{10}$$

$$\mu_{FE} = \frac{2L}{WC_{ox}} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \tag{11}$$

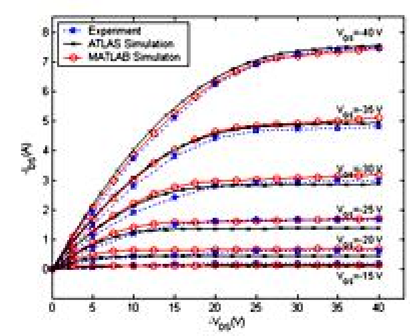

Fig.6: Output characteristic of organic field-effect transistor with PMMA gate insulator obtained from simulation and analytical model results and experiment values

Effective mobility is shown in the third column of the tables 2 and 3 which has been measured in a relatively high current point. Third column of table 2 has been obtained by eq.11 from saturation region of the simulation results. Meanwhile third column of table 3 shows experiment data. These two columns show different values for the mobility and this is the main source of mismatch exists between diagrams of figures 6 and 7, and as mentioned before, it is due to surface roughness which cannot be included in the current simulation software easily.

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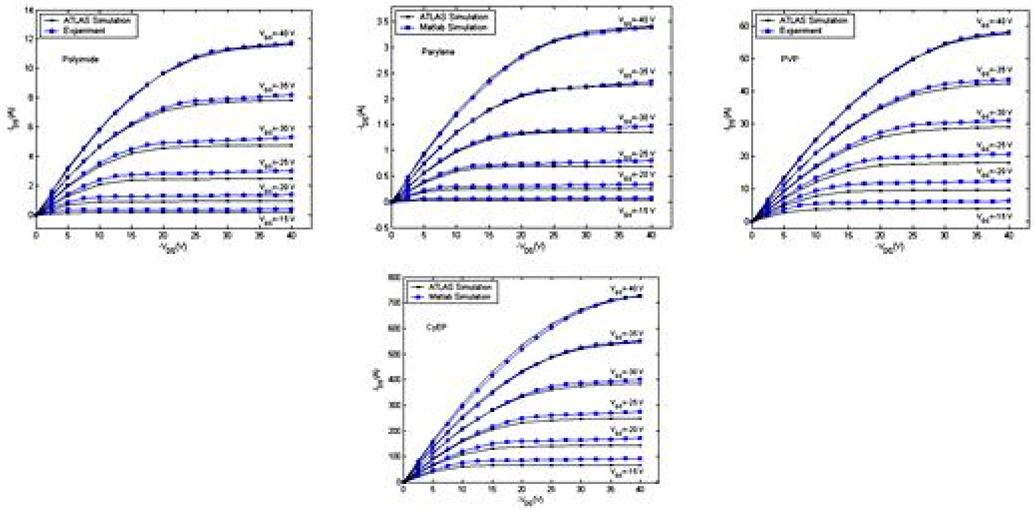

Figure 7: Output characteristics of the studied transistors with simulation and analytical model

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